IN THE SPECIFICATION

Please substitute paragraph 0024 with the following:

[0024] With reference to Figure 3, the disposable poly Ge layer is removed from stack 14; and this may be done, for example, by a H_2O_2 or HNO_3 etching process, while the PFET area is covered by a photo resist. After the poly Ge layer is removed, an ~~as~~ As or P deep ion implantation process is employed to dope the N+ polySi gate 20. The implant goes into the substrate but it is kept sufficiently away from the active device area by the fat spacer. After the N+ polySi gate implantation is performed, the NFET area is then covered by photoresist, poly Ge 22 is removed and Boron deep implantation is performed to dope the P+ polySi gate 20 (not shown).